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Design of RF Power Amplifier for Satellite Ground Station

Saw Kay Thwe Moe[#1], Zaw Min Naing[*2], Kyaw Soe Lwin[#3]

[#]*Department of Electronic Engineering, Mandalay Technological University, Myanmar*
[1]estherr1311@gmail.com
[3]kyawsoelwin007@gmail.com

[*]*Technological University (Maubin), Myanmar*
[2]zawminnaing@gmail.com

***Abstract*— This paper explores the design of RF power amplifier for satellite ground station. The overall circuit for RF power amplifier is implemented in this paper. The circuit is more suitable for C band which covers the range of 4GHz to 6GHz with small signal gain of greater than 10 dB. The goal of this paper is to design a 2W CMOS rf power amplifier in Comtech satellite network. The design is realized with the help of BSIM model (metal oxide semiconductor field effect transistor) platform. The implementation procedure for RF power amplifier is also presented in this paper. This procedure includes preamplifier stage and power amplifier stage. Preamplifier stage includes modeling the transistor design, biasing of that transistor and stability checking analysis. Input and output matching networks were introduced to provide the maximum possible transfer of power between a source and its load. And the power amplifier stage includes design calculation of Class E power amplifier and its tuning procedure. The performance results are evaluated by the Superspice software platform. A good agreement between the measurements and the simulation results is also demonstrated.**

***Keywords*— RF, Power amplifier, BSIM, 5GHz, C band**

I. INTRODUCTION

As communication networks grow in services and higher in quality, new challenges are posed on RF electronics. One of the circuits where this push forward has been mostly sensed is the RF power amplifier, power amplifier, either its hand-held or base station applications. Many applications for power amplifier design are used in broadcast digital television, satellite and military system [1]. Fig. 1 shows typical block diagram of satellite communication system. Radio frequency power amplifier is a key component of communication system. In most RF and microwave power amplifiers, the largest power dissipation is in the power transistor. RF power amplifier consumes most of the power consumption within a transmitter, reducing its consumption power will improve the transceiver performance. It is usually implemented by CMOS or GaAs process for better high frequency performance. As CMOS technology has been greatly improved recently, it is possible to implement CMOS Radio frequency power amplifiers [2].

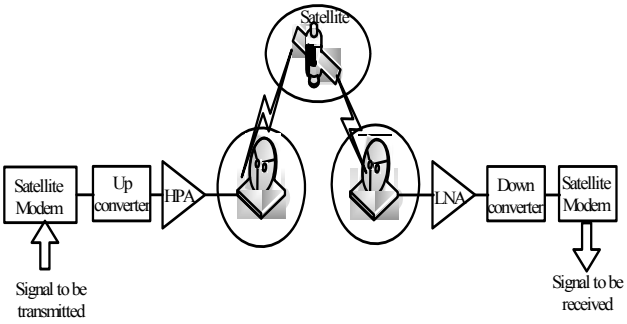

Fig. 1 Typical satellite communication system

This paper introduces C band, CMOS radio frequency power amplifier design. It has the transmitter portion of satellite ground station. It is shown in Fig. 2 with highlighted portion that is intended. In this diagram, the baseband signal is modulated onto a intermediate-frequency carrier which is up-converted to the actual broadcast frequency. It is then amplified as necessary before actually reaching the antenna. The designed structure was used for the power amplifier to obtain the necessary power level and high efficiency. Efficiency is maximized by minimizing power dissipation, while providing a desired output power. The main feature of C band Comtech satellite network for transmitter power amplifier is 2, 5, 10 watts BUC [4]. So, 2 watts CMOS RF PA is intended to design in this paper. It has two main stages: the power amplifier and preamplifier stage. The preamplifier small signal gain has greater than 10 dB. Its design consideration is presented in detail in the next section.

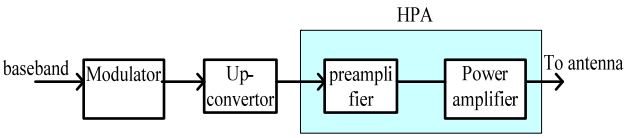

Fig. 2 Block diagram of transmitter potion of the satellite ground station

II. DESIGN CONSIDERATION

RF power amplifier for satellite ground station is considered with three main parts. The first main part is selection of transistor that is used in both preamplifier and power amplifier stages and the second is preamplifier design procedure and the last is power amplifier design consideration.

A. Selection of Transistor

The first and the most important step in power amplifier design are to select a suitable transistor in order to meet the required specifications of an amplifier. In this paper, it is desired to design an amplifier that covers a range from 4GHz to 6GHz. In this design consideration for RF power amplifier, NMOS transistors are used only. BSIM3 model were used to model the performance of the MOS transistor. The model parameters are available in MOSIS' homepage. Due to the luck of modelling information offered the BSIM3v3 data sheet, to extract the minimum set of information necessary for power amplifier design are decided. So, by extracting a set of output V-I characteristics curve for design calculation requirements of power amplifier are begun with software platform. From this simulation, I_D =11.91mA for V_{GS} = 1V as an operating point for this transistor. V-I characteristic curve of BSIM3v3 model is simulated with anasoft platform and transfer characteristic curve is taken from MATLAB environments.

B. Preamplifier Design Procedure

Preamplifier design procedure is considered to the three main parts. To achieve the desired performance, the power amplifier output requires a high peak voltage drive. The required high voltage drive cannot be delivered by the mixer stage or whatever block might precede the PA. Thus, a high gain preamplifier must be designed to deliver the necessary driver level. A high voltage gain of about 10 mandates the intended power amplifier.

1) DC Biasing Network: The amplifier must operate reliably and maintain certain specifications over large temperature extremes, DC bias network must be careful design. In this portion, the design of the DC biasing circuit that isolates RF from DC in the desired bandwidth is discussed. It simply uses voltage divider biasing method. The drain current I_D is 11.91mA at V_{GS} 1V as an operating point for this transistor is chosen. Then the second step is continued to check the stability of this network.

2) Checking of Stability: It is possible to predict the degree of stability of a transistor before the devices in the circuit are actually placed. This is done through a calculation of the Linvill stability factor, C.

$$C = \frac{y_r y_f}{2 g_i g_o - \mathrm{Re}\left(y_r y_f\right)} \tag{1}$$

From the calculation, the value of C is 0.08 where the y parameters are got from the data sheet of BSIM3v3 model. When C is less than 1, the transistor is unconditionally stable at the bias point that has been chosen. So, the next step is continued to design the matching network.

3) Matching Network: Impedance matching is often necessary in the design of RF circuitry to provide the maximum possible transfer of power between the source and the load. Firstly, the ac analysis of this device is done at the design consideration of matching network. The values for ac analysis are taken with the following equations.

$$C_{gd} = -\mathrm{Im}\, Y_{11} / \omega \tag{2}$$

$$C_{gs} = \mathrm{Im}\, Y_{11} / (\mathrm{Im}\, Y_{11})^2 \tag{3}$$

$$C_{ds} = \mathrm{Im}\left[Y_{22}\right] / \omega - C_{dg} - \frac{C_{jd}}{1 + \omega^2 C_{jd}} \tag{4}$$

The required data in the equations can be gotten from the data sheet of BSIM3v3 model. Transconductance values, and gate resistance are calculated with these following equations and the Miller theorem is used.

$$g_m = \mathrm{Re}\left[Y_{21}\right]|_{\omega^2 = 0} \tag{5}$$

$$g_{ds} = \mathrm{Re}\, Y_{22}\,|_{\omega_2 = 0} \tag{6}$$

$$R_g = \mathrm{Re}\, Y_{11} / (\mathrm{Im}\, Y_{11})^2 \tag{7}$$

From calculation with these equations, the input impedance value, Z_{in} = 44.676-j107.10Ω and the output impedance value, Z_{out} = 122.88-j62.053Ω are calculated. In the input matching network, shown in Fig. 3, low pass Pi filter is used and the values are got with the following equations. The input matching network is placed between the source and the active element and these inductance and capacitance values are designed with the Smithchart and these equations. And as this matching network Pi high pass filter is used.

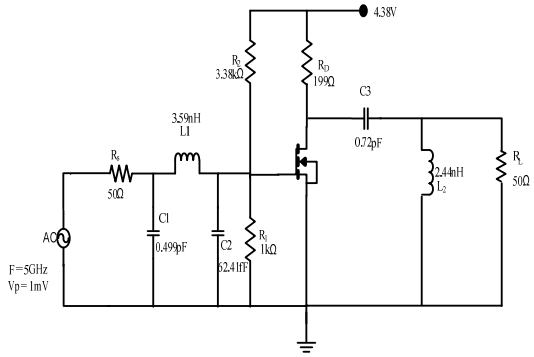

Fig. 3 Preamplifier circuit diagram

$$L_1 = \frac{XN}{N} = 3.59\text{nH} \tag{8}$$

$$C_1, C_2 = \frac{B}{\omega N} \tag{9}$$

C_1 = 0.499pF and C_2 = 62.41fF

In the output matching network, high pass filter is used and these component values are calculated with these equations.

$$C_3 = \frac{1}{\omega XN} = 0.72\ pF \tag{10}$$

$$L_2 = \frac{N}{\omega B} = 2.44\ nH \tag{11}$$

The complete preamplifier circuit diagram is shown in Fig. 3.

A. Power Amplifier Design Consideration

To achieve high gain and high output power, Class E power amplifier was chosen. The circuit diagram of Class E power amplifier stage is shown in Fig. 6. This Class E power amplifier stage is considered with three portions. They are design calculation, checking this design with optimization principles and tuning procedure.

1) Design calculation: In this paper, the transistor is operated as a switch. The amplifier's output power P depends primarily on the collector/drain dc supply voltage V_{CC} and the load resistance R but secondarily on the value chosen for Q_L. This paper includes an accurate equation for P that includes the effect of Q_L. However, the needed component values can be found by numerical methods. The relationship among P, R, Q_L, V_{CC} and the transistor saturation offset voltage V_O by a second- order polynomial function of Q_L is the following equation.

$$R = \left(\frac{(V_{CC} - V_O)^2}{P}\right) 0.576801 \left(1.001245 - \frac{0.451759}{Q_L} - \frac{0.402444}{Q_L^2}\right) \tag{12}$$

The effective dc supply voltage is the actual voltage and in the design V_{CC} is 15V. V_O is zero for field effect transistor. R = 52.29Ω is calculated from the equation. And then the loaded Q_L network that includes C_1, C_2, and L_2 is designed these equations.

$$C_1 = \frac{1}{2\pi fR\left(\frac{\pi 2}{4}+1\right)\frac{\pi}{2}}\left(0.99866 + \frac{0.91424}{Q_L} - \frac{1.03175}{Q_L^2}\right) + \frac{0.6}{(2\pi f)^2 L_1} \tag{13}$$

C1 = 0.1348666pF

$$C_2 = \frac{1}{2\pi fR\left(\frac{1}{Q_L - 0.104823}\right)}\left(1.00121 + \frac{1.01468}{Q_L - 1.7879}\right) - \frac{0.2}{(2\pi f)^2 L_1} \tag{14}$$

C_2 = 0.385799nH

For the case of loaded Q_L network is 3 and the usual choice of X_{L1} being 40 or more times the unadjusted value of X_{C1}, the adjustments for the susceptance of L_1 add 2% or less to the unadjusted value of C_1 and subtract 0.5% or less from the unadjusted value of C_2. So, the RFC or L_1 is 0.299uH. Finally, L_2 is determined by the designer's choice.

$$L_2 = \frac{Q_L R}{2\pi f} \tag{15}$$

L_2 = 4.99406 nH

When calculating the design values, these values must be checked with the following Table I [6]. This table gives normalized exact numerical solutions for output power, C_1 and C_2 for the eight values of Q_L over the entire possible range from 1.7879 to infinity, for the usual choice of D = 50%. When checking these values, tuning procedure as the last portion is considered.

TABLE I
DEPENDENCE OF OUTPUT POWER, C1, AND C2 ON LOADED Q

Q_L	$PR/(V_{CC}-V_O)^2$	$C_1.2\pi fR$	$C_2.2\pi fR$
Infinite	0.576801	0.18360	0
20	0.56402	0.19111	0.05313
10	0.54974	0.19790	0.11375
5	0.51659	0.20907	0.26924
3	0.46453	0.21834	0.63467
2.5	0.43550	0.22036	1.01219
2	0.38888	0.21994	3.05212
1.7879	0.359699	0.21770	infinite

2) Tuning Procedure: The circuit parameters were chosen to meet the requirements of the design via equation 12 through 15. The circuit will operate with the nominal Class E waveform, while delivering a specified output power at the specified frequency, if the chosen parameter values are installed in the actual hardware. Fig. 4 shows a V_{CE} waveform for an amplifier with off nominal tuning. If how changes of L_2 and C_2 will affect that waveform is known, L_2 and C_2 can be adjusted to meet two criteria at operating frequency.

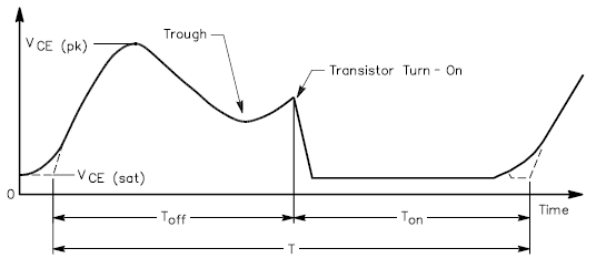

Fig. 4 Typical mistuned V_{CE} waveform

Fig. 5 shows that how L_2 and C_2 affect the V_{CE} waveform. In that case, C_1, C_2, and L_2 can be adjusted to achieve three conditions simultaneously at the operating frequency. There are the desired output power, transistor voltage of $V_{CE(sat)}$ just before transistor turn on and zero slope of the V_{CE} waveform just before turn on.

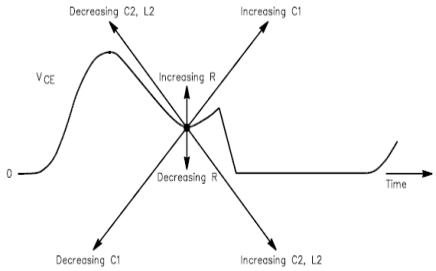

Fig. 5 Effects of adjusting load network components

After the power amplifier stage is considered the design calculation, checking with the reference and adjusting with the tuning procedure, the complete circuit diagram of power amplifier stage can be taken and is shown in Fig. 6.

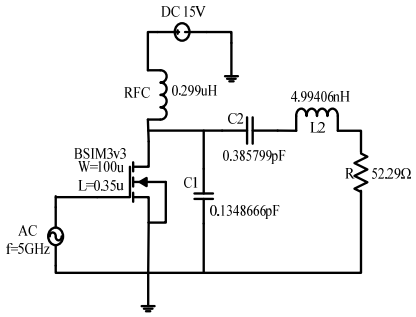

Fig. 6 Power amplifier output stage

III. SIMULATION RESULTS

The preamplifier stage is simulated with superspite software platform. The input power is 1mW (0dBm). When simulating, the output voltage waveform is seen in Fig. 7. And the small signal gain has greater than 10dB. This output is the input of the power amplifier stage.

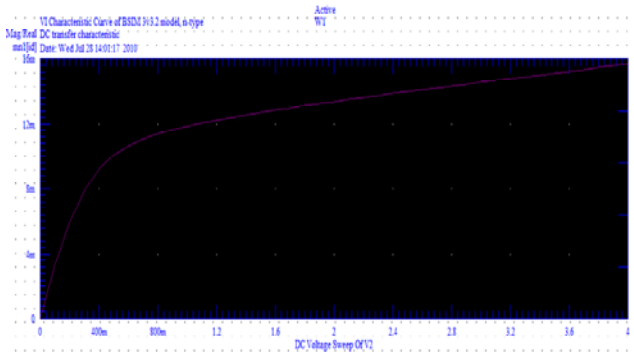

Fig. 7 V-I Characteristic curve of BSIM3v3 model

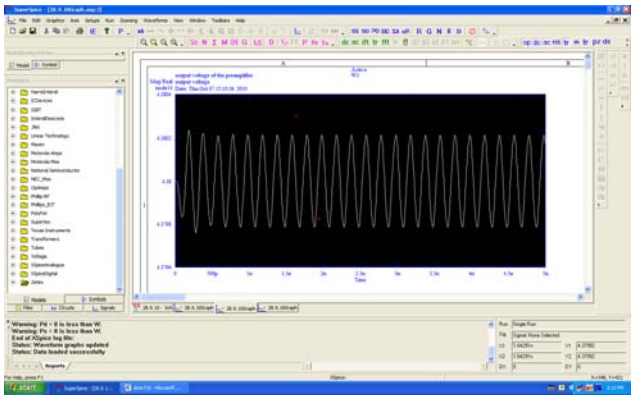

Fig. 7 Output voltage analysis of simulated preamplifier

When the power amplifier stage is simulated with the output of the preamplifier, the output voltage and power waveform curve are seen in Fig. 8 and 9. In power output curve, it can be seen the maximum output power between 4GHz and 6GHz. And its output power is 2 watts (33dBm) that the goal of my research.

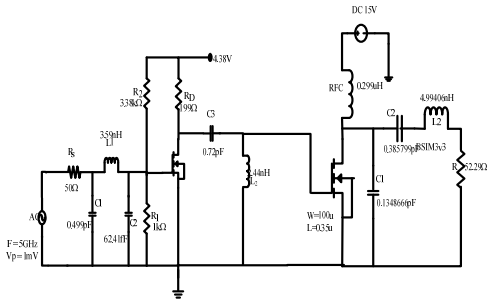

Fig. 8 Complete circuit diagram of RF power amplifier

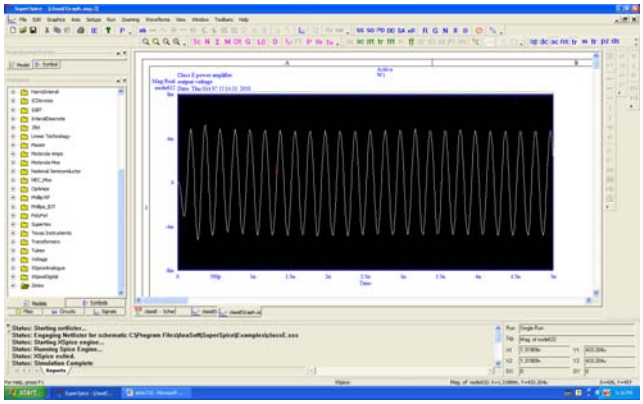

Fig. 8 Output voltage analysis of simulated RF power amplifier

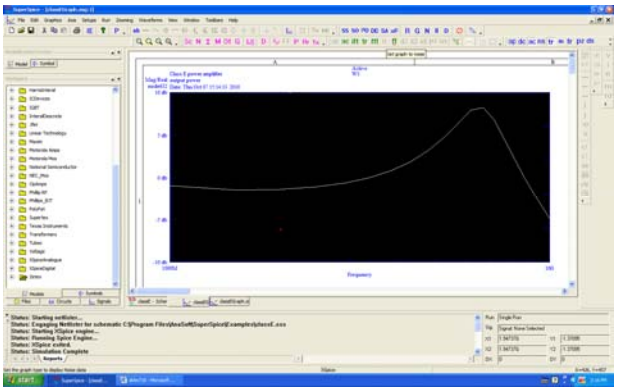

Fig. 9 Output power analysis of simulated RF power amplifier

IV. CONCLUSION

The paper presented C band CMOS RF power amplifier design for satellite ground station. RF power amplifier was designed and simulated in this paper. In designing the RF power amplifier, the main goal is to be stable unconditionally for the complete range of frequencies where the device has a substantial gain. The power amplifier delivers maximum output power and small signal gain has greater than 10dB at 4GHz to 6GHz within C band. Simulation results show that RF power amplifier designed in this paper can be implemented for ground station of Comtech Satellite network. Simulation results show that the output power of complete power amplifier stage could provide maximum output swing (2 watts-33dBm) at the operating frequency 5GHz. And the preamplifier generates the required voltage swing at a node and its 180 degrees shift another node.

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